Two Days National Workshop on VLSI Cadence Tool

Organized by

Department of Electronics,

Kavayitri Bahinabai Chaudhari North Maharashtra University, Jalgaon

In Association with

Entuple Technologies Pvt. Ltd. Bangalore

Date: 22nd and 23rd March 2019

About the University:

The Kavayitri Bahinabai Chaudhari North Maharashtra University, Jalgaon (Formerly known as North Maharashtra University, Jalgaon) established on 15th August 1990 under the Maharashtra Universities Act. The University has opened it's doors of higher education to mostly "first generation learners" of this area. Access, equity and academic excellence are the thrust areas of the University's educational endeavor.

The University was awarded with FOUR STAR grade in the year 2001, B grade with 2.88 CGPA in the year 2009 and A Grade with 3.11 CGPA in 3rd Cycle re-accreditation in year 2015 by National Assessment and Accreditation Council (NAAC), Bangalore.

As per the National Institutional Ranking Framework (NIRF) - 2016 by Ministry of Human Resource Development, Government of India, Kavayitri Bahinabai Chaudhari North Maharashtra University (Formerly known as North Maharashtra University) ranked 59th amongst top 100 Universities and Institutes in India.

About the Department:

The School of Physical Sciences consists of two departments namely, Department of Physics and Department of Electronics. In the academic year 1991-92 the School started its academic activity. In the first year of establishment, the School started a post-graduate program in Electronics under the Department of Electronics.

The Department has been recognized a technologically advanced center for high quality teaching and research to meet the latest requirements of companies and was granted by UGC to run the M.Tech., (VLSI Technology) course under the Faculty of Engineering in the scheme of Innovative Programs in the year 2005.

At present, the Department of Electronics has 05 full time faculty members consisting of 02 Professors and 03 Assistant Professors. It is due to the dedicated efforts of the active faculty members, valuable guidance of the distinguished personalities, timely support of University authorities and un-quenching curiosity and enthusiasm of students, that the Department is progressing to make on National and International arena in its academic pursuits and frontline research.

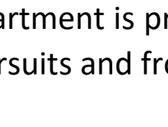
About Entuple:

Entuple is a next generation solutions enabler in cutting edge technologies. Entuple delivers world class simulation solutions in Applied Electromagnetics, Semiconductor (VLSI), System Design & Reliability, Mechanical, CFD and RF. Our product solutions include PCB Prototyping, Planer Antenna prototyping systems. Entuple has developed its own range of semiconductor-based power drives and process control solutions. We cater to wide range of customers in semiconductor, manufacturing, defense and aerospace and academia.

Course Outline:

Day 1 - ***A seminar on VLSI Industry Roadmap and Opportunities:***

- VLSI Industry Global Trends and Indian Perspective
- VLSI and Electronic System Design - An Overview
- Role of academia for ESDM growth in India - Opportunities for Faculty, Research Scholars and young graduates
- VLSI and ESDM flow – An Abstract view and Q & A



WHAT OUR CUSTOMERS SAY:

By attend this training, I will surely show myself a bit higher than others. *--- Harshita Jain, Student, School of Electronics*

Much better experience, because of detailed explanation & long time period of training. *--- Viresg Pandey, Student, SGSITS Indore*

This hands-on workshop programme is very beneficial for getting entry into an industry. *--- Parul Vamney, Student, Shri. G. S. Institute of Tech. & Sci.*

Day 2 - ***A Workshop on VLSI & System Design flow using Cadence, OrCAD, P-spice and PCB:***

Session 1:

- Cadence Design Flow
- Overview of features supported by CentOS and new tools
- Hands-on session - Layout Analysis
- Functional Verification flow using Incisive
- RTL Synthesis and DFT flow using Genus
- PD flow with Innovus that includes:
  Floor Planning, Power Planning, Placement, CTS, Routing, Generation of GDSII
- STA with Tempus
- Static and Dynamic Power Analysis with Voltus
- Logical Equivalence Check with Conformal

Session 2:

FULL CUSTOM DESIGN FLOW:

- Schematic Capture using Virtuoso Schematic Editor
- Functional Simulation using Spectre
- Schematic driven Layout Design using Virtuoso Layout Editor
- Physical Verification which includes DRC and LVS using Assura
- Parasitic Extraction
- Post Layout Simulation
- Generation of GDSII

Who can attend this Workshop?

B.E./M.Sc./M.E./M.Tech. /Ph.D. Students, Teachers and Researchers from Science, Engineering and Technology

Patron:
Prof. P. P. Patil,
Honorable Vice Chancellor,
KBC NMU, Jalgaon

Co-Patron:
Prof. P. P. Mahulikar,
Pro. Vice Chancellor,
KBC NMU, Jalgaon

Chairman:
Prof. D. S. Patil,
Head,
Department of Electronics,
KBC NMU, Jalgaon

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Prof. A. M. Mahajan
Mr. M. S. Netkar
All research students

Resource Persons:
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Business Manager,
Mr. Avinash Keshev
Sr. Application Engineer,
Entuple Technologies Pvt. Ltd.,
Bangalore

Contact Person:
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+91 968754112
umesh.paldhikar@entuple.com

PARTICIPATION FEES STRUCTURE

Category	Fees for Seminar (Day 1)	Fees for Hands-on-Training (Day -2)
Students	100/-	300/-
Faculty	500/-	1000/-
Industrial Delegates	1000/-	1500/-

Venue

VLSI Tools and Simulation Lab
Department of Electronics,
Kavayitri Bahinabai Chaudhari North Maharashtra University,
Umavi Nagar, Jalgaon - 425001
(M.S.) India

NOTE:

- This workshop is non-residential hence; the participants should make their own stay arrangement.
- Participants can register for first day for seminar however, hands-on-training (Day 2) is limited to 36 participants only on first come first serve basis.
- The above mention fee includes working lunch and tea. The fees are nonrefundable in case of last-minute cancellation.
- Certificate will be given to all the participants attending the workshop and to the one's who attend both, workshop followed by hands-on-training.
- Interested participants should submit their application through proper channel on or before 18th March 2019 by 5:00 PM in the format available on University website to Convener(doekbcnmu@gmail.com). Application received after due date will not be entertained.
- For any query the applicant may contact convener or co-convener (doekbcnmu@gmail.com)

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On
"VLSI Cadence Tool"

22nd and 23rd March 2019

Organized by

Department of Electronics

Kavayitri Bahinabai Chaudhari North Maharashtra University, Jalgaon (MS), India

REGISTRATION FORM

- Name: ……
- Designation: ……
- Affiliation: ……
- Address for communication: ……

  ……

  ……
- E-mail: ……
- Phone No.: (O) ……
- Phone No.: (M) ……
- Gender: Male/Female
- Payment of Registration Fees:
- Payment mode: DD/Cash

If paid by DD: DD No: ……

Dated: ……

Issuing Bank:……

Branch:……

Date: Signature of the Applicant

Principal / Head of Institution Seal: